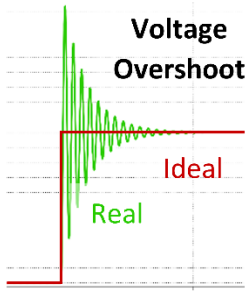
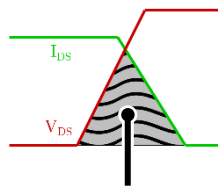
Advanced Switching Cell Design Techniques

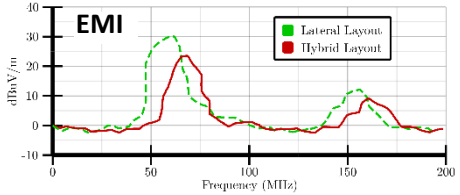
Berkeley Power and Energy Center

Motivation and Application

Power converters operate by switching between different circuit states. Ideally, the switching transitions would be instantaneous and lossless. In reality, parasitic effects cause switching losses, voltage overshoot, and electromagnetic interference. Advanced design techniques are presented here, which mitigate these effects and enable unprecedented performance.







Interleaved Commutation Loop Layout [2]

Commutation loop inductance is critical to switching performance. Advanced layout techniques can be utilized to reduce this inductance.

Interleaved hybrid decoupling capacitor loops with electrically thin vertical bulk capacitor loop

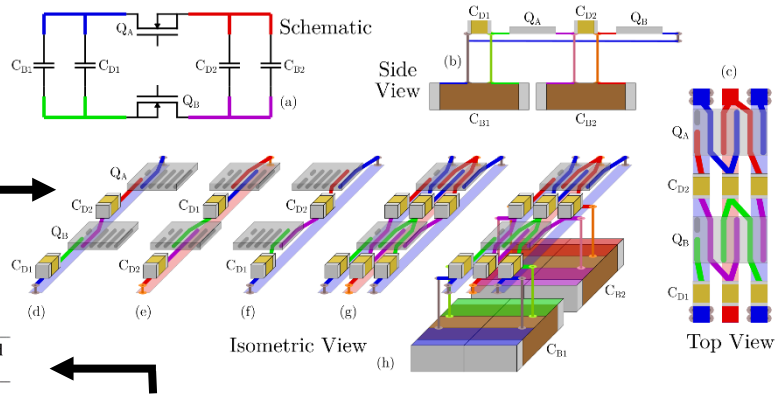
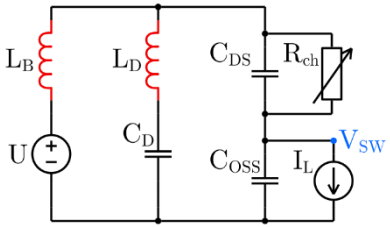


Table 1: Commutation Loop Comparison

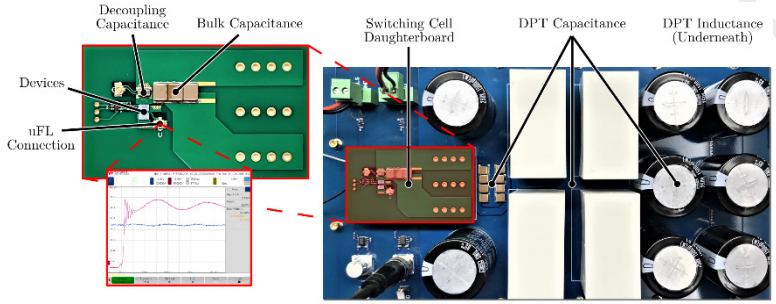
Switching Cell Design	Electrically Thin	Hybrid & E-thin	Hybrid Reference	Proposed Design
Simulated Inductance	1.15 nH	450 pH	521 pH	443 pH
Measured Inductance	2.85 nH	940 pH	—	1.14 nH
Board Area	370 mm²	330 mm²	420 mm²	420 mm²

- Proposed design achieves nearly 3x better performance than best approach without decoupling capacitors
- 20% better than state of the art

Optimal Decoupling Capacitor Sizing [1]

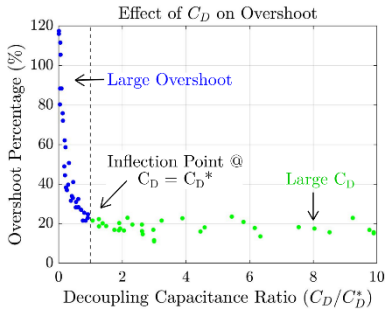


Simplified Switching Circuit Model



Double Pulse Test Hardware Setup

Experimental Data



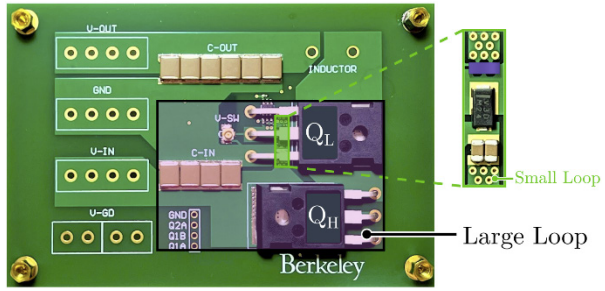
Determined optimal decoupling capacitor size given load current and output capacitance of the device:

$$C_D^* = 10 * \max\{C_{OSS}, 2L_B I_{ML}^2 / U_{ML}^2\}$$

Decoupling Device [3]

For many applications, transistors with large through-hole packages are used, due to their high power handling capability. In this work, a small surface-mount gallium-nitride transistor is added to improve switching performance.

Buck converter hardware prototype



50% reduction in losses

References:
[1] L. Horowitz and R. C. N. Pilawa-Podgurski, "On Decoupling Capacitor Size in GaN-Based Power Converters," 2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL), Tel Aviv, Israel, 2022, pp. 1-5, doi: 10.1109/COMPEL53829.2022.9830000.
[2] L. Horowitz and R. C. N. Pilawa-Podgurski, "Modular Switching Cell Design for High-Performance Flying Capacitor Multilevel Converter," 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 2022, pp. 342-347, doi: 10.1109/APEC43599.2022.9773604.
[3] L. Horowitz, N. M. Ellis and R. C. N. Pilawa-Podgurski, "Decoupling Device for Small Commutation Loop and Improved Switching Performance with Large Power Transistors," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 2620-2624, doi: 10.1109/APEC43580.2023.10131426.

Logan Horowitz | Email: logan_h_horowitz@berkeley.edu