Principal Investigator: Prof. Robert Pilawa-Podgurski

Bio: Robert Pilawa-Podgurski is currently an Associate Professor in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley. Previously, he was an Associate Professor in Electrical and Computer Engineering at the University of Illinois Urbana-Champaign. He received his BS, MEng, and PhD degrees from MIT. He performs research in the area of power electronics. His research interests include renewable energy applications, electric vehicles, energy harvesting, CMOS power management, high density and high efficiency power converters, and advanced control of power converters. Dr. Pilawa-Podgurski received the Chorafas Award for outstanding MIT EECS Master’s thesis, the Google Faculty Research Award in 2013, and the 2014 Richard M. Bass Outstanding Young Power Electronics Engineer Award of the IEEE Power Electronics Society, given annually to one individual for outstanding contributions to the field of power electronics before the age of 35. In 2015, he received the Air Force Office of Scientific Research Young Investigator Award, the UIUC Dean’s Award for Excellence in Research in 2016, the UIUC Campus Distinguished Promotion Award in 2017, and the UIUC ECE Ronald W. Pratt Faculty Outstanding Teaching Award in 2017. He was the 2018 recipient of the IEEE Education Society Mac E. Van Valkenburg Award given for outstanding contributions to teaching unusually early in one’s career. In 2023, he received the UC Berkeley EECS Department Electrical Engineering Outstanding Teaching Award. He is co-author of fifteen IEEE prize papers.
Lab Members:

Dr. Nathan Ellis  
Dr. Samantha Coday  
Margaret Blackwell  
Rose Abramson  
Nathan Brooks  
Kelly Fernandez  
Marrin Nerenberg  
Logan Horowitz  
Tahmid Mahbub  
Rod Bayliss III  
Yicheng Zhu  
Rahul Iyer  
Joseph Schaadt  
Sahana Krishnan  
Jiarui Zou  
Haifah Sambo  
Francesca Giardine  
Ben Liao  
Nathan Biesterfeld  
Elisa Krause  
Nagesh Patle
Ongoing Research Projects
Motivation and Application
- Commercial aviation benefits from electric & hybrid vehicles
- Electric engines can be quieter and cleaner than jet engines
- Electric drive system must be power-dense and efficient
- Advanced power dense motors\(^2\) need low THD, high frequency drive current

**NASA MEA Roadmap**

NOx emissions 80% fuel consumption 60% acoustic noise 71dB

High Power Dynamometer
- Dyno incorporates two low-inductance Emrax 348 machines (peak power: 260 kW)
- Testing validated the Flying Capacitor Multilevel Converter’s (FCML) strength in a realistic motor drive system

Experimental Verification or Other
- Prototype meets NASA performance metrics for turbo-electric aircraft\(^4\)
- Integration of advanced thermal management will boost maximum output power and efficiency
- Modular design provides for power scalability and fault resiliency
- Next steps: verification of floating-point motor control algorithm and high-power dyno and next generation inverter hardware development

<table>
<thead>
<tr>
<th>Peak Efficiency</th>
<th>NASA Target</th>
<th>This Work</th>
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<td>99%</td>
<td>98.95%</td>
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<table>
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<tr>
<th>Power Density</th>
<th>NASA Target</th>
<th>This Work</th>
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<tr>
<td>19 kW/kg</td>
<td>38.4 kW/kg</td>
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</tbody>
</table>

References:

*=rodbay@berkeley.edu Ricky Liou, rliou92@berkeley.edu*
**Proposed Solution**

- Regulating boost DC-DC converter facilitates varying battery voltage and inverter load demand

**Motivation and Application**

- Air travel accounts for ~200 million tons of CO₂ emissions annually (3% of US greenhouse gas emissions)[1]
- Air travel demand is expected to double every fifteen years
- Electrification of flight requires efficient, lightweight, and reliable power conversion
- Hardware must be flight qualified

Pictured: Ampaire Electric EEL flight

**Hardware Prototype**

- Snubbers enable decreased overlap loss without sacrificing conduction path
- Paralleled switches enable increased areal power density
- Derated energy density metric used to optimize flying capacitor part/count
- Custom inductor achieves 3x mass reduction

**Modeled Performance**

- \( \#X \) = number of parallel switches

Loss Breakdown

- \( P_{\text{cond}} \) (39%)
- \( P_{\text{core}} \) (2%)
- \( P_{\text{winding}} \) (12%)
- \( P_{\text{gate}} \) (10%)
- \( P_{\text{ESR}} \) (1%)
- \( P_{\text{on/off}} \) (5%)

\[ 1 \text{ https://www.epa.gov/greenvehicles/fast-facts-transportation-greenhouse-gas-emissions} \]
Motivation and Application

- Air travel accounts for ~200 million tons of CO₂ emissions annually (3% of US greenhouse gas emissions)[1]
- Air travel demand doubles every fifteen years
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Air travel accounts for ~200 million tons of CO₂ emissions annually (3% of US greenhouse gas emissions)[1]
Air travel demand doubles every fifteen years
Electrification of flight requires efficient, lightweight, and reliable power conversion

FCML with Optimal Passive Component Selection

Capacitor Sizing
- Conventional approach utilizes large, identical capacitors
- Proposed approach optimally selects unique capacitors for each flying capacitance
- Enables > 50% reduction in size

Hardware Prototype

- 10 kW, 800 V, 14-level FCML
- Sandwich-style layout with two printed circuit boards
- Ultra-thin design, only 8 mm thick!

Experimental Verification

- Highest power density among state-of-the-art aircraft inverters
- Excellent capacitor balancing and low output distortion despite the small size of the converter

References:
Tethered Power Systems for Lunar Mobility and Power Transmission (TYMPO)

Motivation and Application
Extreme terrain capable robots will enable further exploration on sites such as pits on the moon and Martian landscape. Tethered power systems have been proposed to power these small rovers; however, they require high voltage DC power [1].

Challenges
High voltage switches are difficult to use in space due to radiation effects. Additionally, the high voltage conversion ratio makes it difficult to design a compact and efficient power converter. Therefore, multilevel topologies offer promising solutions [2].

System Architecture (Flying Capacitor Multilevel Converter)
- Comparison of cascaded structure consisting of resonant flying capacitor multilevel converter (FCML) and regulating FCML (resonant FCML + regulating FCML) vs single-stage FCML converter
- Bus capacitance requirement diminishes benefits of cascaded structure

Passive Mass Minimization
- Comparison of 8-level regulating mode FCML converter with a resonant mode FCML converter, demonstrating the advantages of a resonant converter in terms of passive component mass
- Each converter operating point is optimized for minimal mass based on the peak energy storage requirements of the passive components

Hardware Verification
840 V-to-120 V space-rated FCML converter to verify:
- PCB structure (Gate drive daughterboard)
- Part selection
- Thermal solutions
- Mass optimization

References:

TyPMO architecture
Lander
DC-DC Step-up
Tether
DC-DC Step-down
Rover

Tethered rover to explore lunar pits

FCML converter schematic

Estimated mass breakdown of cascaded FCML converter structure

Student: Elisa Krause, Maggie Blackwell, Logan Horowitz
Email: {elisa_krause, blackwell, logan_h_horowitz}@berkeley.edu
Capacitor Volumetric vs. Gravimetric Energy Density

\[ \rho_V = \frac{2CV^2}{V} \quad \text{[J/mm}^2\text{]} \]

\[ D(V, C) = \frac{\text{Mass}}{\text{Vol}} \]

\[ \rho_G = \frac{2CV^2}{\text{Mass}} \quad \text{[J/mg]} \]

Use Specific Density (D) to Derive Gravimetric Energy Density from Volumetric Energy Density

Enabling Buck-Type AC/DC Grid-Tied Rectifiers Using Flying Capacitor Multi-Level Converters with Advanced Control

Motivation and Application

Data center power consumption 1%+ of global electricity demand and growing [1]

Single-stage rectification
- Increased efficiency
- Greater power density

240 V_{ac} 

FCML and Active Flying Capacitor Voltage Balancing

6-Level Buck-Type FCML PFC Rectifier
- Reduced magnets volume
- High FOM switches

Control Schematic

Hardware

12-level FCML Converter Inductor Output Capacitors

- 12-level prototype reconfigured as 5-level converter
- Flying capacitor voltages measured with non-isolated instrumentation amplifier

Experimental Verification

Power Factor
- Target 0.97
- Passive Balancing 0.88
- Active Balancing 0.97+

References:

Rod Bayliss III Email: rodbay@berkeley.edu

Background and Motivation

**Existing** two-stage lateral power delivery (LPD) architecture
- Large power distribution network (PDN) and high PDN losses
- Occupies a large area on the top side of the baseboard

**Proposed** single-stage vertical power delivery (VPD) architecture
- Much lower PDN losses
- Saves the topside area for high-speed communication and memories

Advantages of Switching-Bus-Based Architecture
- Does not require a large decoupling capacitor to maintain a stiff DC bus voltage
- One redundant switch can be removed on each switching bus while two stages are merged
- Ensures complete soft-charging operation

Proposed Switching Bus Converter (SBC)

**Hybrid switched-capacitor topology**
- Two 2-to-1 switched-capacitor (SC) front-ends
- Four series-capacitor buck (SCB) modules
- Two switching buses

**Hardware prototype**
- Good modularity
- Custom four-phase coupled inductor
- Efficient and compact gate drive circuitry

Experimental Results and Performance Comparison
- 92.4% peak system efficiency and 607 W/in³ power density (including gate drive loss and volume)

Thermal image at equilibrium with 220 CFM air cooling (I_{out}=1200 A)
- Measured 48-V-to-1-V efficiency
- Performance comparison between this work and the state-of-the-art 48-V-to-1-V hybrid SC works

References:

Yicheng Zhu, Ting Ge, Nathan M. Ellis, and Jiarui Zou
Email: {yczhu, gting, nathanmilesellis, jiarui.zou}@berkeley.edu
Motivation and Application

- 90-240 Vac to 400 Vdc is a critical conversion stage for applications such as data center power delivery, electric vehicle charging, etc.
- Ac-dc power factor correction
  - Reduce boost inductor size
- Twice-line frequency power ripple buffering
  - Reduce buffer capacitor size

Design Objectives

High Power Density

- Reduce system volume via new circuit topologies and control

Reduced Weight

- Custom 3D-printed cold-plate (collaboration with Miljkovic Group at UIUC)
- 3D printed cold-plate
- Printed Fluid Channels

Hardware Implementation

Flying capacitor multi-level* (FCML) converter as the power factor correction stage

- Use of flying capacitors as energy storage greatly decreases volume of passive components and reduce filtering needs
- Series-stacked Buffer as energy buffer stage
  - Use of active circuitry decreases capacitance requirement for twice-line frequency buffering and further promoted volume reduction

Experimental Verification

- Peak tested power: 6.1 kW
- Peak efficiency (1.1 kW): 99.1%
- Efficiency @ 6.1 kW: 97.8%
- PFC up to 1.5 kW: > 99.6%
- Box-volume power density with cold plate: 7.6 kW/L

References:


Kelly Fernandez, Rahul Iyer, Jiarui Zou
Email: kefernandez@berkeley.edu, rkiyer@berkeley.edu, Jiariui.zou@berkeley.edu
An EMI-Compliant and Automotive-Rated 48 V-to-PoL Dickson-Based Hybrid Switched Capacitor DC-DC Converter

Motivation and Application
Data center power delivery and automotive powertrains tending towards a 48 V distribution rail
- Higher intermediate bus voltages minimize losses and reduce cabling weight
This work demonstrates the merit of hybrid SC topologies for use in 48 V automotive systems
- Regulating Dickson-based hybrid SC topology
- EMI mitigation techniques – filtering and spread-spectrum frequency modulation

Topography and Challenges
Hybrid switched-capacitor, 8-to-1 interleaved-input, single-inductor Dickson converter
- Differential input → continuous input current → reduced required input filter
- Inductor at output → filtering and EMI shielding at low side
- Inductor at output → voltage regulation
Challenges
- Split-phase switching necessary for soft-charging of the flying capacitors
- Automotive component selection
- High efficiency, power density, and CISPR 25 Class 5 EMI compliance

Hardware Implementation
Uses only automotive-qualified parts
Switch selection based on required function, both Si and GaN
EMI input filter and spread spectrum frequency modulation (SSFM) to reduce EMI

Experimental Results
Differential Mode (DM) EMI results

References:

References:
Bidirectional Power Transfer in Hybrid Switched-Capacitor Converter for 48V/12V Regulated Automotive Applications

**Motivation and Application**

Bidirectional DC-DC Converter

- **48V battery**
- **12V battery**

**Need:**
- 48V battery should be able to deliver **extra power** to 12V battery based on increased load demand and vice-versa.

**Challenges:**
- Delivery of **high current** with **high efficiency** and **high power density** in both directions

**Converter Topology**

- 48V-to-12V **regulated** cascaded hybrid resonant-PWM converter [1]
- 1st stage uses a conventional doubler in resonant mode
- 2nd stage used two interleaved doublers operating in PWM mode.

**Advantages of Proposed Control Technique**

- Implements Natural Balancing of all flying capacitors.
- Achieves Soft-charging and soft-switching.
- Minimizes the size of the intermediate capacitor $C_{mid}$.

**Hardware Demonstration and Results**

- Measured Efficiency at:
  - Input voltage: 48 – 60V
  - 80 A full-load current
  - Regulated 12 V output

- 80A, 99% peak eff. 3115 W/in³ power density
- 21% loss and 63% size reduction over SOTA
A General Approach for Design Optimization of High-Performance Hybrid Switched-Capacitor Converters

Motivation and Application

Hybrid switched-capacitor converters
- More capacitive energy storage than inductive energy storage for size reduction
- Multiple low-voltage switches in place of a single high-voltage switch for efficiency improvement

Topology Comparison
- Analytical method to compare relative size and performance of various topologies
- Include the impacts of capacitor voltage ripple and inductor current ripple on passive component volume and switch stress

Passive Component Volume and Switch Stress Trade-Off

Increasing the switching frequency beyond resonance
- Trading ↑ switching loss for ↓ conduction loss

Increasing capacitance beyond minimal volume
- Trading ↑ volume for ↓ VA rating (efficiency)

Impacts of Switching Frequency and Conversion Ratio on Minimal Passive Volume [1]

- Series-Parallel has smaller passive volume → Higher power density
- Increasing $\Gamma = \frac{f_{SW}}{f_{RES}}$ → smaller passive volume → Higher power density

Validation of Analytical Model

Passive component volume for varied capacitance to validate minimal volume method

References:
Simplified circuit model and general output impedance model

Modeling Derivation and Effect Analysis

Background and Motivation

- Insufficient terminal capacitances can greatly affect converter efficiency
- Bulky terminal capacitors become the bottleneck of converter miniaturization

Modeling Derivation and Effect Analysis

Simplified circuit model and general output impedance model

Multi-Resonant Compensation Control (MRCC)

- Challenge: zero current switching (ZCS) is not achievable with 0.5 duty ratio with small $C_{in}$
- Solution: ensure ZCS operation with the optimal duty ratio and switching frequency
- Result: 5x terminal capacitance reduction without harming efficiency

Simulation and Experimental Verification

Key considerations

- Minimize switching loss
- Accurate parameter acquisition

High accuracy

References:


Effect of terminal capacitances

Inductor current waveform of a 2-to-1 pure SC converter with different terminal capacitances

Inductor current waveform of a 2-to-1 ReSC converter with different terminal capacitances

Output impedance of a 2-to-1 resonant SC converter with different $C_{in}$ and $C_{out}$

Output impedance of a 2-to-1 pure SC converter with different $C_{in}$ and $C_{out}$

(a) Schematic

(b) Hardware prototype

(a) Phase 1                        (b) Phase 2

Circuit model of a pure SC converter with $C_{in}$ and $C_{out}$

Circuit model of a ReSC converter with $C_{in}$ and $C_{out}$

(a) Phase 1                        (b) Phase 2

Inductor current waveform of the conventional control. (c) Inductor current waveform of MRCC.

(a) Comparison of output impedance. (b) Inductor current waveform of the conventional control. (c) Inductor current waveform of MRCC.

Simulation and Experimental Verification

(b) Hardware prototype

Multi-Resonant Compensation Control (MRCC)

• Challenge: zero current switching (ZCS) is not achievable with 0.5 duty ratio with small $C_{in}$
• Solution: ensure ZCS operation with the optimal duty ratio and switching frequency
• Result: 5x terminal capacitance reduction without harming efficiency

References:

Motivation and Application

- Dickson-based converters are popular for hybrid switched capacitor (SC) solutions due to the reduced switch stress as compared to other topologies [1]
- Applications: high-conversion ratio systems
  - 48 V bus architectures for data centers and automotive powertrains
- Transistor switching losses can be significant share of overall losses, especially with trends towards faster switching frequencies
- Soft-switching techniques, such as zero-current and zero-voltage switching (ZCS and ZVS) can be used to reduce these losses

Challenges

- Phase-timings become non-trivial to determine
- ZVS timings are also non-trivial
  - Non-linear switch output capacitance
  - Multiple switches with different blocking voltages

References:

**Motivation and Application**

Data Center Two-Stage Power Architecture

Due to finite terminal filtering capacitances, the efficiency of ReSC converters is often maximized when they are precisely soft switched [4]. However, circuit nonidealities render ZCS and ZVS timing challenging to estimate creating the need for active control techniques.

- Class II MLCC DC Bias Derating
- Inductor Soft Saturation

**Theory and Control**

Non-Ideal ZCS

Non-Ideal ZVS

By sensing the switch node voltage, nonideal soft switching conditions can be detected. Complete ZCS or ZVS can then be achieved by implementing the proposed control scheme.

**Control Flowchart**

- Convergence to soft switching can be achieved from a wide range of initial switching frequencies.
- Active ZVS and ZCS control allow for higher peak efficiencies than the conventional openloop techniques.

**Experimental Verification**

- Convergence to soft switching can be achieved from a wide range of initial switching frequencies.
- Active ZVS and ZCS control allow for higher peak efficiencies than the conventional openloop techniques.

**Hardware**

The presented 2-to-1 converter is the foundational ReSC topology. The control technique is verified on a 48-V-to-24-V hardware prototype and can be extended to higher conversion ratio topologies.

**References**:  


**Bias Derating**

**Excessive inductor current**

**Insufficient inductor current**

**Active ZVS and ZCS control**

**Convergence to Soft Switching**

**Convergence of Phase 1**

**Convergence of Phase 2**

**Increase duration of Phase 1**

**Increase duration of Phase 2**

**Decrease duration of Phase 1**

**Decrease duration of Phase 2**

**Position of Phase 1**

**Position of Phase 2**

**Switch node voltage above**

**Switch node voltage below**

**Efficiency vs. Output Current**

**Students:** Haifah Sambo, hsambo@berkeley.edu

Yidong Zhu, yidong@berkeley.edu

Post-doc: Ting Ge, tingge@berkeley.edu

Nathan Miles Ellis, nathanmilesellis@berkeley.edu
Motivation and Application

Hybrid Switched Capacitor (HSC) power converter topologies are being adopted in 48V to point-of-load (PoL) applications. Within the HSC converter class, Dickson-type converters [1] achieve the lowest Volt-Amp switch stress, indicative of a smaller semiconductor footprint for equivalent performance. However, some of these topologies require a non-conventional clocking scheme — recently coined as “split-phase switching” [2] — to ensure high efficiency is preserved. Executed in parallel with complimentary work in [3], this work presents a closed-loop split-phase control appropriate for regulating PoL converters [4]; over-coming a key obstacle to the deployment of a new and highly competitive class of hybridized power converter topologies.

Closed-loop Split-phase Control Demonstrated in Hardware

An added Split-Phase Control Loop detects “hard-charging” events and informs appropriate phase timing adjustments within a conventional FPGA-based clock generator.

Example: Phase Progression of the SDIH (Dickson-Type) Converter

The duration of all phases are fully constrained as a function of $V_{IN}$, $V_{OUT}$, $I_{IN}$, $f_{SW}$, & component values. The practical inclusion of loss and component derating/mismatch necessitates continuous and dynamic phase duration adjustments.

Experimental Verification

- **Closed-Loop Control**
- **Theoretical Timings**
- **Without Split-Phase Control**

**Operating Point**
- $V_{IN} = 48V$
- $V_{OUT} = 3.3V$
- $f_{SW} = 300$ kHz

Dr. Nathan Ellis, Haifah Sambo - Email: nathanmilesellis@berkeley.edu

Active Soft-Charging Control for Hybrid and Resonant Switched-Capacitor Converters

Motivation and Application
Dickson-derived converters are increasingly used for both fixed-ratio and direct-to-PoL applications in the datacenter and transportation space. They can achieve very low switch stress (i.e. Volt-Amp product), which means that lower-voltage (and therefore less lossy) switches can be used compared to other topologies for a given output power.

Split-Phase Control
Certain Dickson topologies require more complex split-phase control schemes [1] in order to achieve full soft-charging of all fly capacitors. Split-phase control timings can be complex to calculate and vary depending on component tolerance, circuit non-idealities, and operating condition, necessitating active control [2], [3].

Capacitor Losses: Hard-Charging vs. Soft-Charging


Phase 1 Split-Phase Operation
If the (1a,1b) and (2a,2b) transitions occur at the wrong time, hard-charging occurs, resulting in current spikes and discontinuous capacitor voltages.

These voltage steps can be sensed, allowing the controller to auto-tune split-phase times to achieve soft-charging operation.

Experimental Verification

• An 8-to-1 resonant Dickson converter was used for validation.
• The control scheme was able to converge on soft-charging split-phase timings when 1) initialized in a hard-charging condition, and 2) when enabled during load step transients.

Smooth capacitor voltages signify soft-charging operation.

References:

Analog Sensing Circuitry

• The analog circuitry is flexible in implementation, and stages can be combined into single package op-amps or off-loaded into internal microcontroller comparator units to increase density.

Experimental Verification

• An 8-to-1 resonant Dickson converter was used for validation.
• The control scheme was able to converge on soft-charging split-phase timing when 1) initialized in a hard-charging condition, and 2) when enabled during load step transients.

Smooth capacitor voltages signify soft-charging operation.
Closed-Loop Balancing Control and Capacitor Voltage Estimation for the Flying Capacitor Multilevel Converter

Balancing Control Motivation

Open-loop balancing of capacitor voltages is unreliable

• Capacitor voltages during large-signal transients exhibit underdamped dynamics
• Peak switch stress may be greater than $\frac{V_{in}}{N-1}$ and can cause switch overvoltage in high-performance designs using low-voltage switches

Natural Balancing

Capacitor Voltage Estimation

• Active balancing requires measurement of capacitor voltages
• Measuring each capacitor voltage with its own differential sensor is expensive
• Can instead measure switched-node voltage with single-ended sensor and calculate capacitor voltages
• Solve system of equations iteratively with reduced computation burden
• Demonstrated on industry-standard Texas Instruments C2000 DSP

Experimental Verification

• Active balancing ensures capacitor voltages track nominal values during supply transients
• Single-sensor estimation of capacitor voltages is reliable and low-cost

Closed-Loop Control

• Model average behavior of FCML converter to obtain “plant” for control
• Structure of plant informs controller design: duty ratios can be controlled differentially to steer capacitor voltages
• Balancing controller runs in parallel with controller(s) regulating load voltage
• Closed-loop system is decoupled – controllers operate without mutual interaction

References:
A Hybrid Switched-Capacitor Solar Microinverter Utilizing a Fixed-ratio Resonant DC-DC Stage and Flying Capacitor Multi-level DC-AC Stage

Motivation and Application

Hybrid Switched-Capacitor Converters

- The Cascaded Series-Parallel converter (CaSP) has been used as a power-dense dc-dc step-down solution in the 48V application space but is being adapted use as a boost stage [1].
- The flying capacitor multilevel converter (FCML) can be used to step down the

Rooftop solar requires efficient and power dense solutions to convert power for use in homes and at the grid.

System Architecture

- Three sub-intervals of one switching cycle, each with a unique resonant LC tank impedance [2].
- Achieves ZCS, partial ZVS.
- Can be used as stand-alone startup circuitry.
- 400V to 240Vac. Voltage at output of inductor is rectified sine wave that is unfolded by H-bridge.
- HV buffer allows for reduction of capacitance due to smaller current ripple

Hardware

- CaSP System Specifications
  - 35-40V input
  - 350-400V, 500W output
  - System able to produce 240 Vac output at light load
  - CaSP achieves ZCS during full system operation at 240 Vac output

- FCML System Specifications
  - 350-400V input, 500W+
  - Sensing for control included on this board.
  - 2nd revision coming soon

Experimental Validation

- Rooftop solar requires efficient and power dense solutions to convert power for use in homes and at the grid.
- System able to produce 240 Vac output at light load
- CaSP achieves ZCS during full system operation at 240 Vac output

References:


Peak efficiency with 255 Vac output at light load: 93.5%
A Charge Injection Loss Compensation Method for a Series-Stacked Buffer to Reduce Current and Voltage Ripple in Single-Phase Systems

Motivation and Application

The Series-stacked buffer (SSB) is an active buffer topology that achieves high energy utilization and greatly decreases the power conversion system volume without compromising efficiency [2]. However, there can be a large amount of residual ac current ripple on the dc bus due to SSB’s control methodology that injects real power through the reactive buffer branch. This control is required to charge the $C_2$ capacitor in the SSB that acts as a dc source for a full-bridge converter. Specifically, this ripple gets worse in applications with low source impedance, such as battery systems.

Proposed “Charge Injection” Method

The Charge Injection method has a separate branch that handles real power delivery while the rest of the SSB handles the reactive power buffering. As a result, the dc-link current ripple is greatly reduced.

Hardware

Component | Part No. | Parameters
---|---|---
$S_1$ – $S_4$ | EPC2033 | 150 V, 6 mΩ
$S_{CI}$ | GaN Systems GS66506T | 600 V, 2 A
$D_{CI}$ | ON Semiconductor MURS160T3G | 650 V, 67 mΩ
$L_{CI}$ | Coilcraft MSS1210-104 | 100 μH
$C_1$ | TDK B32524Q1686K000 | 100 V, 68 μF x 3
$C_2$ | TDK B32776G4406K000 | 450 V, 40 μF x 2

The real power injection causes large ac current ripple along the dc-link. (24% ac current ripple shown at 1.5 kW at 400 Vdc).

Experimental Verification

The peak-to-peak ac current ripple is reduced:
- By maximum of 5.3x
- And average of 4.3x
- 3x at peak load

Charge Injection method achieves an average efficiency of 99.4% across all loads.

References:


Student Name: Kelly Fernandez, kefernandez@berkeley.edu
Utilizing Harmonic Injection to Reduce Energy Storage in a Single-Phase Active Energy Buffer

Motivation

• Single-phase power converters rated for high power applications require reactive buffering on the dc bus to maintain a constant and clean dc power input or output. Often this is a bulky electrolytic capacitor.

• [1] found that buffer storage requirements for a passive buffer could be reduced 56% for the addition of allowable 3rd and 5th harmonics.

• We apply this harmonic injection method for energy storage reduction in the capacitors of the series-stacked buffer (SSB), which is a power-dense alternative to the conventional capacitor solution.

Challenges and Control

• Determining the expected voltage ripple on each of the capacitors is nontrivial.

• Figure out how to control an active buffer when additional harmonics are added to the system.

Circuit Topology and Hardware

The SSB is an active buffer that combines a primary energy buffer capacitor with an H-bridge. This permits a larger voltage ripple across the main energy storage capacitor maximizing the amount of energy buffered, and subsequently the energy utilization ratio [2].

Experimental Verification

55% reduction in required energy storage split between two capacitors. In an example case, $C_1$ can be reduced from $60\mu F$ to $34\mu F$, and $C_2$ from $27\mu F$ to $20\mu F$ for same dc-bus voltage ripple [3].

References:
Advanced Switching Cell Design Techniques

Motivation and Application

Power converters operate by switching between different circuit states. Ideally, the switching transitions would be instantaneous and lossless. In reality, parasitic effects cause switching losses, voltage overshoot, and electromagnetic interference. Advanced design techniques are presented here, which mitigate these effects and enable unprecedented performance.

Interleaved Commutation Loop Layout [2]

Commutation loop inductance is critical to switching performance. Advanced layout techniques can be utilized to reduce this inductance.

Interleaved hybrid decoupling capacitor loops with electrically thin vertical bulk capacitor loop

| Table 1: Commutation Loop Comparison |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| Switching Cell Design        | Electrically Thin            | Hybrid E-thin              | Hybrid Reference            | Proposed Design              |
| Simulated Electr Inductance  | 1.15 nH                     | 450 pH                     | 521 pH                     | 443 pH                      |
| Measured Electr Inductance   | 2.85 nH                     | 960 pH                     | —                          | 1.14 nH                     |
| Based Area                   | 370 mm²                     | 330 mm²                    | 420 mm²                    | 420 mm²                     |

• Proposed design achieves nearly 3x better performance than best approach without decoupling capacitors
• 20% better than state of the art

Optimal Decoupling Capacitor Sizing [1]

Determined optimal decoupling capacitor size given load current and output capacitance of the device:

\[
C_D^* = 10 \times \max\{C_{OSS}, 2L_{BL} I_{ML}^2 / U_{ML}^2\}
\]

Decoupling Device [3]

For many applications, transistors with large through-hole packages are used, due to their high power handling capability. In this work, a small surface-mount gallium-nitride transistor is added to improve switching performance.

References:
Concluded Research Projects
(with potential follow-up
work in planning stages)
High-Performance 48-to-12 V Cascaded Multi-Resonant Switched-Capacitor Converter for Datacenters

**Motivation and Applications**

- The intermediate bus converter in 48 V data center application requires high efficiency and high power density
- Regulation and isolation are not required

**Proposed Topology**

- Cascaded Multi-Resonant converter
- 1st stage uses only two switches to save space of active components, and gate drive level shifters

**Hardware Demonstration**

- Dimensions: 17.3 × 23 × 6.6 mm
- Power density: 6000 W/in³ at 12 V output
- 80 A continuous output and 130 A - 2 ms transient output

**Experimental Results**

- Measured efficiencies including gate drive loss

**Reference:** T. Ge, Z. Ye and R. C. N. Pilawa-Podgurski, “A 48-to-12 V Cascaded Multi-Resonant Switched Capacitor Converter with 4700 W/in³ Power Density and 98.9% Efficiency,” 2021 IEEE ECCE.
High Performance Single-phase Ac-dc Conversion with Advanced Topology and Control

Motivation and Application

- 90-240 Vac to 400 Vdc is a critical conversion stage for applications such as data center power delivery, electric vehicle charging, etc.
- Ac-dc power factor correction
  - Reduce boost inductor size
- Twice-line frequency power ripple buffering
  - Reduce buffer capacitor size

Hardware Implementation

90-240 Vac to 400 Vdc, 1.5 kW PFC converter

- Single DSP TMS320F28377D for the proposed system control
- GaN System and EPC GaN FETs used in FCML and SSB for high efficiency

Challenges and Solutions

- The boost inductor size is reduced flying capacitor multilevel (FCML) topology
- An active buffer topology - series-stacked buffer (SSB) is implemented to reduce the buffer capacitor for twice-line frequency power ripple buffering

Topologies

- PFC+SSB Coupled Control:
  - PFC Multi-loop control: high-bandwidth “inner” current & low-bandwidth “outer” voltage loop
  - PFC Partial feedforward cancels the input voltage disturbances to input current caused by smaller boost inductor in FCML
  - Buffer control obtains phase and amplitude information from PFC

Control

Experimental Verification

- Total box-volume power density: 230 W/in³
- Peak efficiency: 98.9%
- 1.5 kW efficiency: 98.1%
- THD: < 5%
- Power factor: > 0.994

References:

High Efficiency High Power Density
Hybrid/Resonant Switched-Capacitor Converter

Theoretical Analysis

Swing VA rating
Total passives volume

Practical Challenges and Solutions

Floating gate drive
Capacitor voltage balancing

Systematically analyze and calculate switch and passive utilization
Compare and select the most suitable topology depending on application and power level
Develop control technique to achieve soft-charging and soft-switching

Cascaded Resonant Converter

Two-phase interleaved design
Zero voltage switching technique

Overcome the intermediate decoupling challenge of doubler topology
Operate the tank in the inductive region to achieve ZVS, while improving tolerance of component variations

Experimental Verification

Switch VA rating
Total passives volume

References:
[3] Z. Ye, Y. Lei and R. C. N. Pilawa-Podgurski, “A resonant switched capacitor based 4-to-1 bus converter achieving 2180 W/in3 power density and 98.9% peak efficiency,” APEC 2018

Student: Zichao Ye. Email: yezichao@berkeley.edu
An 83mA 96.8% Peak Efficiency On-Chip 3-Level Boost Converter with Full-Range Auto-Capacitor-Calibrating Pulse Frequency Modulation (ACC-PFM)

Motivation and Applications

- Voltage step-up
- High integration
- Power efficient

High voltages are demanded to:
- Generate efficacious stimulations for bio-implantable devices
- Interface between low-voltage energy harvesters and batteries for wireless sensor network (WSN)
- Program memories for high operational speeds
- Drive LED strings efficiently

Challenges and Solutions

- Topology: 3-level Boost Converter
- Control: ACC-PFM

- ACC-PFM is an integrated controller solution for both V_{OUT} regulation and capacitor balancing

Chip Implementation

- TSMC 65nm CMOS process
- 2.5V devices for 5.0V operation

Measurement Results

- Peak Efficiency: 96.8%
- Input Voltage: 0.3 – 3V
- Output Voltage: 2.4 – 5V
- Peak Output Current: 83 mA
- Peak Switch Current Density: 300 mA/mm²
- Switching Freq.: 0.5M – 45MHz

Excellent performance for wide-range voltage and load variation required in step-up applications, compared to prior arts.

References:

Wen-Chuen Liu, Pei Han Ng, Robert C.N. Pilawa-Podgurski, “An 83mA 96.8% Peak Efficiency 3-Level Boost Converter with Full-Range Auto-Capacitor-Calibrating Pulse Frequency Modulation”, IEEE Custom Integrated Circuits Conf. (CICC), 2019.

Student: Wen-Chuen Liu  Email: joseph.wcliu@berkeley.edu
A 94.2%-peak-efficiency 1.53A direct-battery-hook-up hybrid Dickson switched-capacitor DC-DC converter with wide continuous conversion ratio in 65nm CMOS

Motivation and Application
Increased power density of advanced CMOS nodes in embedded applications requires the power converters to have:
- Higher efficiency to extend the battery life
- Low loss to ease the thermal management
- Higher power density to match the technology
- Maintain performance at large conversion ratios

Typical Battery voltage 3.2 V to 4.2 V
Typical Load voltage 300mV to 1 V
Typical Load current several mA to several A

Challenges and Solutions
Utilized hybrid switched-capacitor (SC) converters.
Switched-Capacitor stage:
- Higher efficiency at large conversion ratios
- Lower rated devices for advance CMOS integration
- Poor regulation

Magnetic Buck stage:
- Achieve tighter regulation
- Lower voltage swing for smaller magnetics

Need higher utilization of passive and active devices:
- Dickson SC has good switch utilization and poor capacitor utilization
- Soft-charging through split-phase control increases capacitor utilization, enhances efficiency and lower switching frequency
- Smaller passives for faster transient response and tighter control

Experimental Verification
Maintained efficiency and power density:
- Across large conversion ratios
- Across large load current range


Hardware
- Implemented in CMOS 65nm bulk process
- Flip-Chip packaging for low parasitic
- Voltage borrowing gate drive to eliminate bootstrap capacitors and increase power density
- Active capacitor balancing and output regulation
- External flying capacitors and inductor
- High density interposer for uModule assembly

System Architecture
- Implemented in CMOS 65nm bulk process
- Flip-Chip packaging for low parasitic
- Voltage borrowing gate drive to eliminate bootstrap capacitors and increase power density
- Active capacitor balancing and output regulation
- External flying capacitors and inductor
- High density interposer for uModule assembly

Increasing Gap
Motivation and Applications

- Multi-layer ceramic capacitors (MLCCs) are a key enabling technology for high density power converters.
- Real losses in MLCCs can be reduced to equivalent series resistance (ESR).
- Data sheets do not provide loss information for realistic operating conditions.

Hardware Implementation

- ESR is dependent on frequency, DC bias, AC amplitude, temperature and harmonic content.
- A circuit was designed to be able to adjust frequency, current amplitude and DC bias of a high harmonic content waveform in order to test the effect on ESR.

Challenges and Solutions

\[ P_{\text{diss}} = \frac{1}{T_{\text{final}}} \left( k_{\text{oil}} \Delta \text{temp} + \int_0^{T_{\text{final}}} \frac{\text{temp}_{\text{oil}} - \text{temp}_{\text{amb}}}{R} \, dt \right) \] [1]

- Measuring loss with electrical characterization is accurate under desired operating conditions.
- A calorimetric method was implemented in order to accurately observe change in ESR.

Experimental Results

- With increased DC bias, the ESR linearly increases, this has been shown with several dielectric types as well as manufacturers.

References:

Capacitor Manufacturer | Capacitor Derating (at 400 V) | ESR increase (at 400 V, 125 kHz)
--- | --- | ---
TDK | 80% | 200%
Knowles | 82% | 243%
Kemet | 72% | 142%
Hybrid Switched-Capacitor DC-DC Converters with Isolation

Motivation and Applications
- Hybrid switched-capacitor converters offer high power density but have been restricted to non-isolated applications
- Traditional isolation methods require bulky and heavy transformers
- Capacitive isolation presents a power-dense alternative to magnetic isolation
- Flying capacitors with high voltage rating act as isolation capacitors

Challenges and Solutions
- ZVS theoretically possible, but not successful at higher input voltages
  - Ongoing issue; we’ll spend more time investigating timing
- Light-load oscillations that damage converter at higher voltages
  - Current solution: avoid light load

Theory of Operation
- Capacitively isolated hybrid switched-capacitor converter based on [1], [2]
- Complete soft-charging of capacitors eliminates loss from transient inrush currents
- 50% duty cycle and two-phase operation
- Switch voltage stress independent of load

Experimental Results
- 94.1% peak efficiency, 2,010 W/in³ power density

Proposed Method and Result

- **2-phase coupled inductors**: schematic, core structure, current waveforms, and flux densities

- **Total flux is proportional to core size and calculated by**:

\[
\phi_{1,\text{max}} \quad \phi_{2p} = \frac{L_s}{K L_s L_s} \left[ L_{1p} + L_{2p} \right] / N
\]

\[
\phi_{\text{sum,N}} = \frac{\phi_{\text{sum,SW,N}}}{V_{\text{out}}} = \frac{4}{\alpha (1 - K)} D + \frac{3}{2}
\]

α: ripple factor, defined by the peak-to-peak inductor current over the maximum dc current

**Reference**: T. Ge, R. Abramson, Z. Ye, and R. C. N. Pilawa-Podgurski, "Core Size Scaling Law of Two-Phase Coupled Inductors – Demonstration in a 48-to-1.8 V Hybrid Switched-Capacitor MLB-PoL Converter," 2022 APEC.

Experimental Results

- Modeled \( \Phi_{\text{sum}} / \Phi_{\text{sum,0}} \) versus \(-K\) at \(\alpha = 0.3\)

- **Converter specifications**

<table>
<thead>
<tr>
<th>Converter specifications</th>
<th>Efficiency at 48 V</th>
<th>Power density &amp; Dimensions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. ( V_{\text{in}} )</td>
<td>48 V</td>
<td></td>
</tr>
<tr>
<td>Max. ( V_{\text{out}} )</td>
<td>1.8 V</td>
<td></td>
</tr>
<tr>
<td>Max. D</td>
<td>0.3</td>
<td></td>
</tr>
<tr>
<td>Max. ( I_{\text{out}} )</td>
<td>65 A</td>
<td></td>
</tr>
<tr>
<td>( f_{\text{sw}} )</td>
<td>250 kHz</td>
<td></td>
</tr>
<tr>
<td>( \alpha )</td>
<td>0.3</td>
<td></td>
</tr>
</tbody>
</table>

**Converter performance summary**

- **Measured efficiency including gate drive loss**

- The converter with coupled L achieves 0.4% higher peak efficiency and 44% higher power density compared to the discrete counterpart.

Hardware Implementation

- **Core size scaling law of two-phase coupled inductors**

\[
\phi_{\text{sum,0}} / \phi_{\text{sum,N}} \text{ versus } -K \text{ at } \alpha = 0.3
\]

- **55% core size reduction by using -0.75 coupling**

- **Multi-Level Binary (MLB) hybrid switched-capacitor converter for 48 V to PoL conversion**

- In Point-of-Load (PoL) applications, inductors usually occupy >50% total volume

- **A general core-size model** is desired to evaluate the duty-ratio advantage of hybrid converters and guide magnetic design

- **Modeled \( \Phi_{\text{sum}} / \Phi_{\text{sum,0}} \) versus \(-K\) at \(\alpha = 0.3\)**

**Converter performance summary**

- **Efficiency at 48 V**

- **Power density & Dimensions**

**Converter specifications**

- **Efficiency at 48 V**

- **Power density & Dimensions**

**Measured efficiency including gate drive loss**

**Reference**: T. Ge, R. Abramson, Z. Ye, and R. C. N. Pilawa-Podgurski, "Core Size Scaling Law of Two-Phase Coupled Inductors – Demonstration in a 48-to-1.8 V Hybrid Switched-Capacitor MLB-PoL Converter," 2022 APEC.

**Ting Ge, Rose Abramson Email:** {gting, rose_abramson}@berkeley.edu
Challenges and Solutions

Traditional data center power factor correction (PFC) units boost voltage before rectification and step-down. **Proposed**: A one-stage single-phase ac-dc converter (240 Vac to 48 Vdc) with PFC

<table>
<thead>
<tr>
<th>Metrics</th>
<th>Existing</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Efficiency</td>
<td>94 %</td>
<td>97.8 %</td>
</tr>
<tr>
<td>Power Density</td>
<td>0.33 kW/L</td>
<td>7.5 kW/L</td>
</tr>
</tbody>
</table>

**Traditional Data Center Architecture**
- Displacement current from $C_{ww}$ and $C_{ff}$ leads to a phase shift in the input current, degrading the power factor. Our improved control algorithm compensates for this current to improve power factor [1].
- Converter will buck or boost depending on point in AC input line cycle.
- Flying capacitor voltages vary with ac line cycle → unique challenges with capacitor balancing.

**Operating Waveforms**
- Preliminary prototype tests buck functionality, so that the converter is off when $|V_{in}| < V_{out}$.
- The converter relies on a stiff 48 V at the output (i.e. the UPS).

**Efficiency Curves**
- Efficiency 94.8% at 240 Vac, 250 W

**Performance Specifications**
- Efficiency 94.8% at 240 Vac, 250 W
- Volume (Box) 2.45 in³
- Power Density 163 W/in³ (w/o heatsink)
- 79 W/in³ (w/ heatsink)

**References**

**Experimental Verification**
- Converter will buck or boost depending on point in AC input line cycle.
- Preliminary prototype tests buck functionality, so that the converter is off when $|V_{in}| < V_{out}$.
- The converter relies on a stiff 48 V at the output (i.e. the UPS).

**Hardware Prototype**
- Current Compensation to Improve Power Factor
- Numbers of Levels 6
- Switching Frequency 40 kHz
- Output Current 4.5 A

**Motivation and Application**
- Traditional data center power factor correction (PFC) units boost voltage before rectification and step-down.
- **Proposed**: A one-stage single-phase ac-dc converter (240 Vac to 48 Vdc) with PFC.
Motivation and Application
Floating switches need floating power supplies
- Typically use isolated power supply for each switch
- Large volume (due to isolation transformer) and high cost

“Cascaded bootstrap” proposed for reduced volume and cost

Challenges with Bootstrap Solution and Innovations
Voltage drops in bootstrap diodes require supply significantly higher than gate-drive voltage
- Local regulation necessary for driving GaN-FETs at 5-6V

Replace bootstrap diodes with FETs
- Reduced voltage drop, bidirectional power delivery

Charge-Pump Technique
Oscillator driven charge pump: can be easily integrated with existing isolated drivers

Can operate at low duty ratios with reduced gate-drive supply
- Higher gate drive efficiency

Experimental Verification
Reduced gate-drive supply with high-side switches fed by charge-pump

References:
Design and Implementation of a (Flying) Flying Capacitor Multilevel Converter

**Motivation and Application**

- DC-DC boost regulation stage added to hybrid electric drive-train architecture to allow variable battery voltage and peak inverter operation.
- Partnered with Ampaire and ARPA-E for flight qualification of hardware.

**Challenges and Solutions [2]**

- Start-up auxiliary circuit and control allows for safe start-up at high voltages.
- Careful shutdown control of FCML is demonstrated as to not over stress switches.
- DC-DC boost regulation stage added to hybrid electric drive-train architecture to allow variable battery voltage and peak inverter operation.
- Partnered with Ampaire and ARPA-E for flight qualification of hardware.

**Hardware Implementation [1]**

- 10-level FCML design is light-weight and compact.
- Modified electrically thin commutation loop design decreases parasitic inductance.

**Experimental Results [3]**

- Measured efficiency (including gate drive losses).

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Samantha Coday, Nathan Ellis
Email: {scoday, nathanmilesellis}@berkeley.edu